REMARKS/ARGUMENTS

Reexamination of the captioned application is respectfully requested.

A. SUMMARY OF THIS AMENDMENT

By the current amendment, Applicants:

1. Thank the Examiner for the acknowledgment of the claim for priority and receipt of the certified copy of the priority document.
2. Thank the Examiner for the consideration and citation of all the references submitted with the Information Disclosure Statement filed on February 13, 2004.
3. Thank the Examiner for allowance of claims 2 – 9.
4. Editorially amend the specification.
5. Editorially amend independent claim 1 and claims 2 – 4, 6 - 8.
6. Respectfully traverse all prior art rejections.

B. PATENTABILITY OF THE CLAIMS

Claim 1 stands rejected under 35 USC 102(b) as being anticipated by U.S. Patent 4,855,614 to Maitre. The prior art rejection is respectfully traversed for at least the following reasons.

The rejection of claim 1 as allegedly being anticipated by Maitre (US Patent 4,855,614) is respectfully traversed. The Applicant submits that Maitre fails to disclose or even remotely suggest each and every limitation claimed. In order for the Examiner to set forth a viable rejection based on anticipation, it is necessary that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Vedregaal Bro. v. Unio Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). (MPEP § 2131).

Maitre generally discloses a switching apparatus for switching input signals so that either signal 1 at input 1 in Fig. 3 or signal 1B at input 1B is presented at the output loading stage 4 (see line 65, col. 2 to line 6, col. 3). The switching is accomplished by using a control voltage signal applied at port 9 (see lines 48-52, col. 2). More specifically, as can be seen in Fig. 4, each path of the switching circuit (top and bottom half of Fig. 4) comprises an input 1 (1B), two transistors T1, T2 in series (T1B and T2B) constituting an amplifying stage, and an impedance matching circuit (comprising C1, L1, C8 with corresponding elements for the bottom half), see lines 36-57, col. 3. The collectors of transistors T2 and T2B are connected at common point 10, which represents the output of the device.

The above switching operates as follows: A control voltage signal is applied at port 7. A more detailed description of the control signal generation is shown in Fig. 6 and explained in lines 10-15, col. 5. When the voltage at terminal 9 in Fig. 6 is high, then transistors T5 and T7 are conducting , which consequently causes transistor T1 of the top path in Fig. 4 to conduct and therefore causes the input signal at port 1 to be present at the output point 10, in contrast to the bottom path (related to port 7B) which is blocked from the corresponding input signal. When the voltage at terminal 9 is low the above process is reversed.

In summary, the switching circuit of Maitre, shown in Figs. 3, 4 and 6, allows the selection of an input signal from a first or a second input port for amplification and presentation to an output port.

The Examiner has identified port 5 (connected to point 10) of Fig. 4 (not Fig. 3 as indicated in the Office Action) as the first port connected to a first device; T2 as the second port connected to a second device that exchanges a signal with the first port, T1 as the third port to which another switching apparatus is cascade connected; and an impedance circuit that reads on the claim language, and corresponding to elements C1, C8, L1.

It is respectfully submitted that the Office Action's arguments are incorrect for at least the following reasons:

a) T2 is not a port to which a second device is connected, a device which exchanges a signal with the device connected to the first port 5. T2 is simply a transistor, which constitutes the second phase in the amplifying stage of one of the two signal paths in the switching circuit of Fig. 3, denoted by "3" therein. Ports in Fig. 4 are 1, 1B, 6, 6B, 7, 7b and 5, not the intermediate transistors T1, T2, T1B, T2B.

b) T1 is not a third port to which another switching apparatus is cascade-connected. First, there is only one switching apparatus in Fig. 4, not two which are cascade-connected. Second, as explained above, T1 is a transistor which constitutes the first phase in the amplifying stage of one of the two signal paths in the switching circuit of Fig. 3, denoted by "3" therein, and not a port.

c) the impedance circuit connected to the left of transistor T1 is conducting when an "ON" signal is applied to the control port 7, and not conducting when an "OFF" signal is applied to the control port 7. This has nothing to do with a cascade-like connection with a second switching apparatus.

The switching device of Maitre is completely different from that of independent claim 1. Whereas the former is concerned with switching between two input signals to provide an amplified output signal, Applicant's device is related to a multiple-stage circuit for interconnecting multiple input signals with multiple receivers, and comprising multiple switching stages. Maitre's circuit has only one switching stage and there is no teaching or suggestion for cascading multiple such stages. Hence, it is respectfully submitted that Maitre does not anticipate claim 1 since it does not disclose the limitations "a second port to which a second device that exchanges a signal with the first device is connected; a third port to which another switching apparatus is cascade-connected, wherein the impedance circuit provides an impedance according to a connection state of the third port, and is electrically disconnected from a signal path when the other switching apparatus is cascade-connected to the third port." Therefore, it is respectfully submitted that the prior art rejection of independent claim 1 be withdrawn.

The Office Action has indicated that claims 2-9 are allowable over the prior art of record. Therefore, it is respectfully submitted that said claims are allowable for at least the limitations contained therein.

C. MISCELLANEOUS

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

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